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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,066	06/24/2003	Satoshi Matsuda	008312-0304355	1198

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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,066	MATSUDA ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,5,6,8 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,5,6 and 8* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06242003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Objections

1. Claims 2 and 6 are objected to on the basis of a lack of clarity in the recitation of limitations regarding gate side wall insulating films. In Claim 2, for example, Applicant recites the presence of a "*gate side wall insulating film formed on a side surface of said gate electrode and on a side surface of said second insulating film*," while in Claim 6, Applicant recites, "*said gate side wall insulating film comprises: a third side wall portion formed on the side surface of said second insulating film portion, and a fourth side wall portion formed on a side surface of said third side wall portion.*" There is no clear definitive identification of side wall portions one through four, and in particular, side wall portions one and two. Correction and/or clarification is required. For the purposes of examination, Examiner will assume that Applicant is referring to insulating layers rather than distinct side wall layers.

Claim Rejections – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2, 5, 6, and 8 are rejected under 35 U.S.C.103(a) as being unpatentable over Curello US 6,503,844 B2) in view of Shell et al. (US 5,429,956).

4. Regarding Claim 2, Curello discloses a semiconductor device comprising:

a semiconductor substrate (40) (Figure 3C) (Col. 4, line 4).

a pair of first diffusion layers (64,66) formed within said semiconductor substrate,

a gate insulating film including a first insulating film portion (42) formed on that portion of said semiconductor substrate which is positioned between said first diffusion layers (64,66) and a second insulating film portion (a lower portion of 60) positioned on both edges of said first insulating film portion (68), and having a thickness (vertical) larger than first insulating film (42) portion.

a gate electrode (44) having a first gate portion (narrow region) formed on the first insulating film portion (42) and a second gate portion (wide region) formed on the second insulating film portion (60), in which the first and second gate portions (44) are formed of the same material (polysilicon) (Col. 4, line 13),

a gate side wall insulating film (an upper portion of 60) formed on a side surface of said gate electrode and on a side surface of said second insulating film portion.

Curello does not disclose the presence of a second diffusion layer formed apart from said first diffusion layers within that portion of said semiconductor substrate positioned below said first insulating film portion. Shell et al. disclose the formation of a diffusion layer (40) (Figure 9) formed apart from said first diffusion layers (62) within the region below the insulating film. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the implant procedures of Shell et al. with Curello to produce a device with improved circuit performance (Shell et al. Col. 3, lines 62 – 67).

5. Regarding Claim 5, Curello discloses a semiconductor device comprising a pair of extension

regions (the end portions of regions [64,66] that are formed directly under the upper portion of layers [60]) formed below said gate side wall insulating film, and a pair of source-drain regions (64,66) formed in contact with said extension regions.

7. Regarding Claim 6, Curello discloses a semiconductor device wherein said gate sidewall insulating film comprises:

a third side wall portion (60) formed on a side surface of said gate electrode and on the second insulating film portion and

a fourth side wall portion (62) formed on a side surface of said third side wall portion.

8. Regarding Claim 8, Curello discloses the presence of an interlayer insulating film (62) formed to surround said gate side wall insulating film with an upper surface substantially equal to an upper surface of said gate electrode, (wherein the upper (vertical) surface of 62 is equal to the upper (vertical) surface of gate electrode 54).

Claim Objections

9. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record do not reasonably teach or suggest, either singularly or in combination,

A semiconductor device wherein a second diffusion layer is formed apart from the first diffusion layers and the "conductivity type of the said second diffusion layer is opposite the conductivity Type of said semiconductor substrate."

Response to Arguments

11. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusions

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's acting supervisor, **Stephen Loke**, can be reached on **(571) 272-1657.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
June 16, 2005

Steven Loke
Primary Examiner

Steven Loke